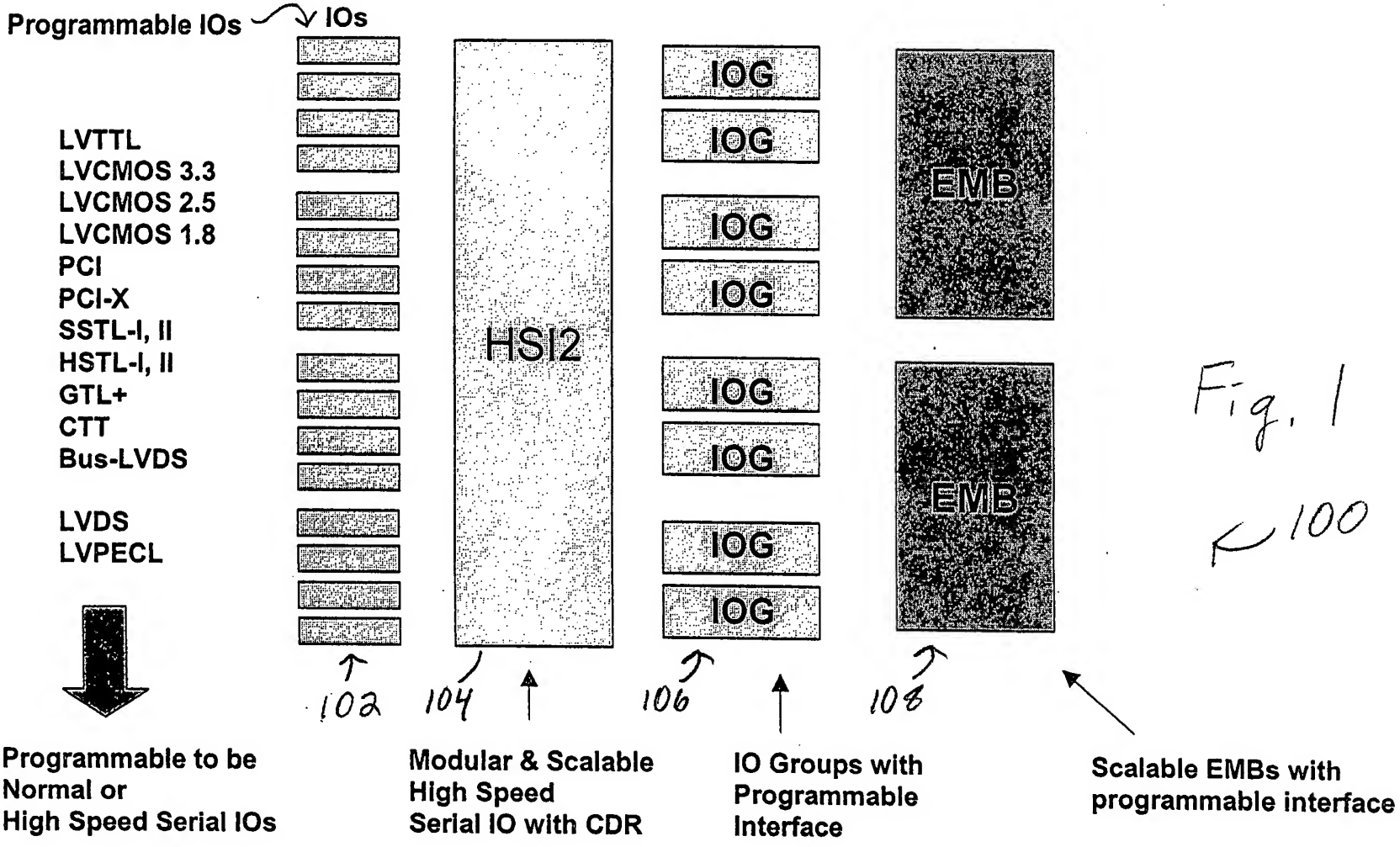

Programmable IOs
IOs
LVTTL
LVCMOS 3.3
LVCMOS 2.5
LVCMOS 1.8
PCI
PCI-X
SSTL-I, II
HSTL-I, II
GTL+
CTT
Bus-LVDS
LVDS
LVPECL
HSI2
IOG
IOG
IOG
IOG
IOG
IOG
IOG
IOG
EMB
EMB
102
104
106
108
IOs Programmable to be Normal or High Speed Serial IOs
Modular & Scalable High Speed Serial IO with CDR
IO Groups with Programmable Interface
Scalable EMBs with programmable interface

Fig. 1

100

HSI2 Block -- Twin SERDES with CDR & CSPLL

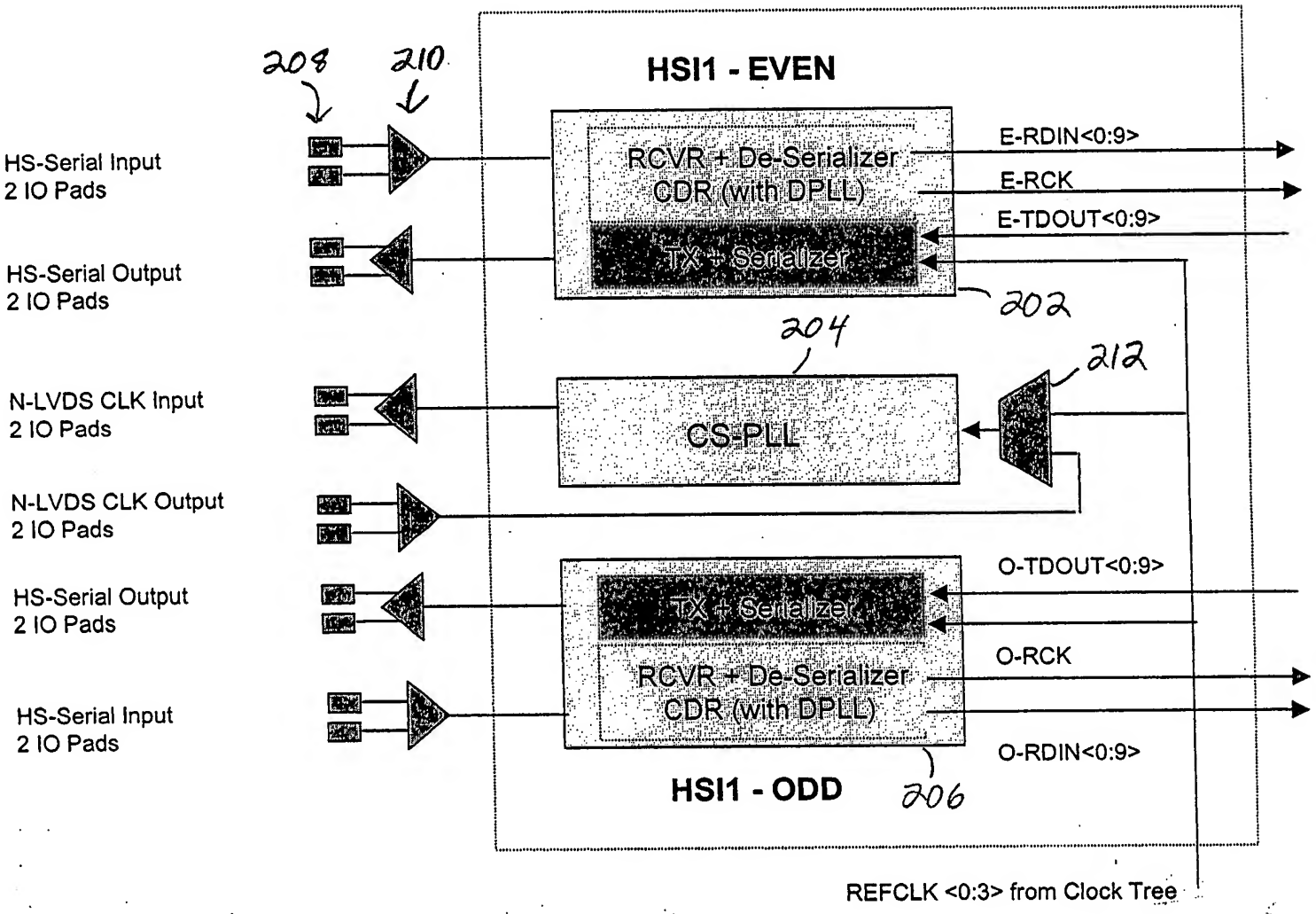
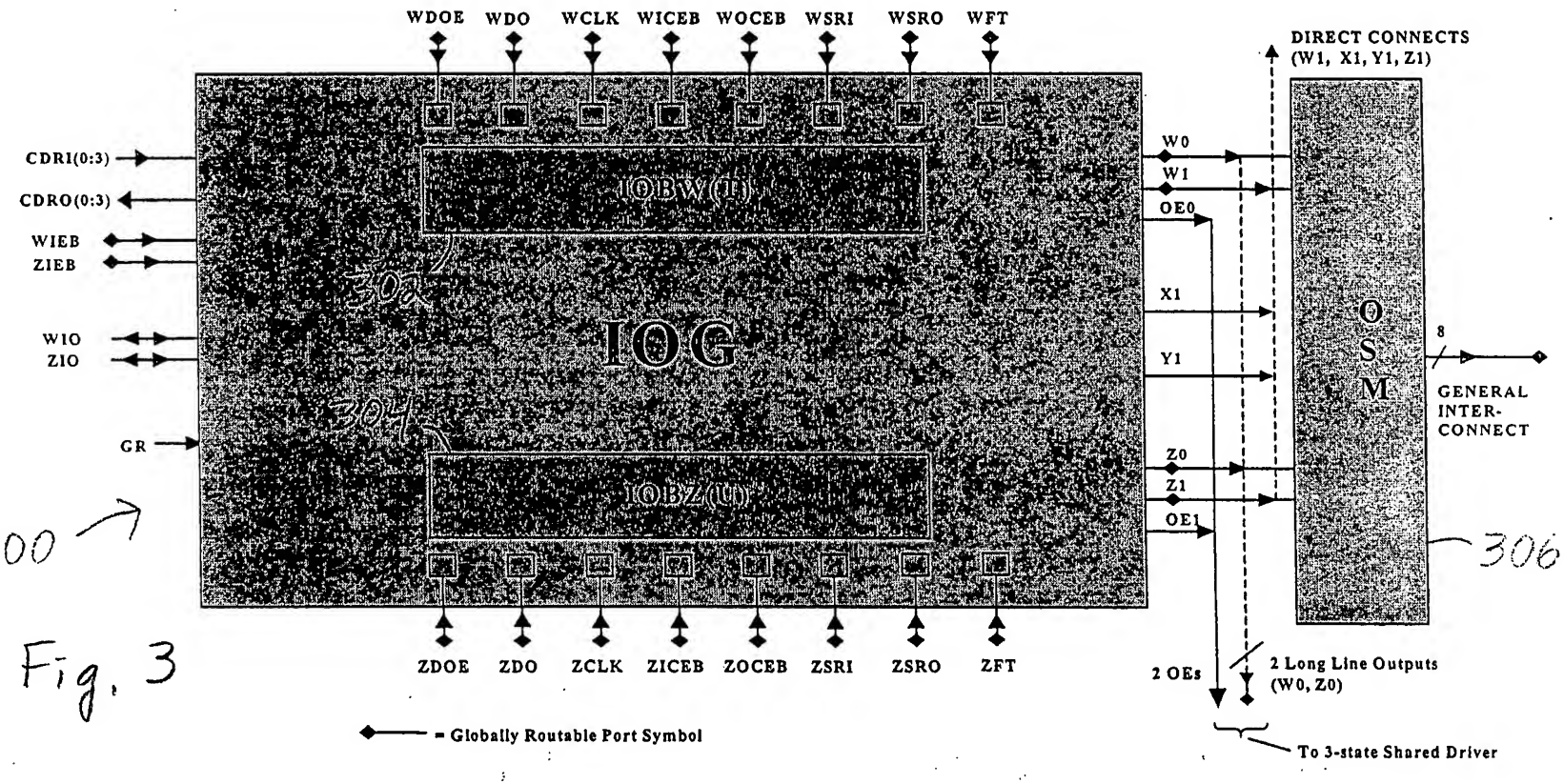


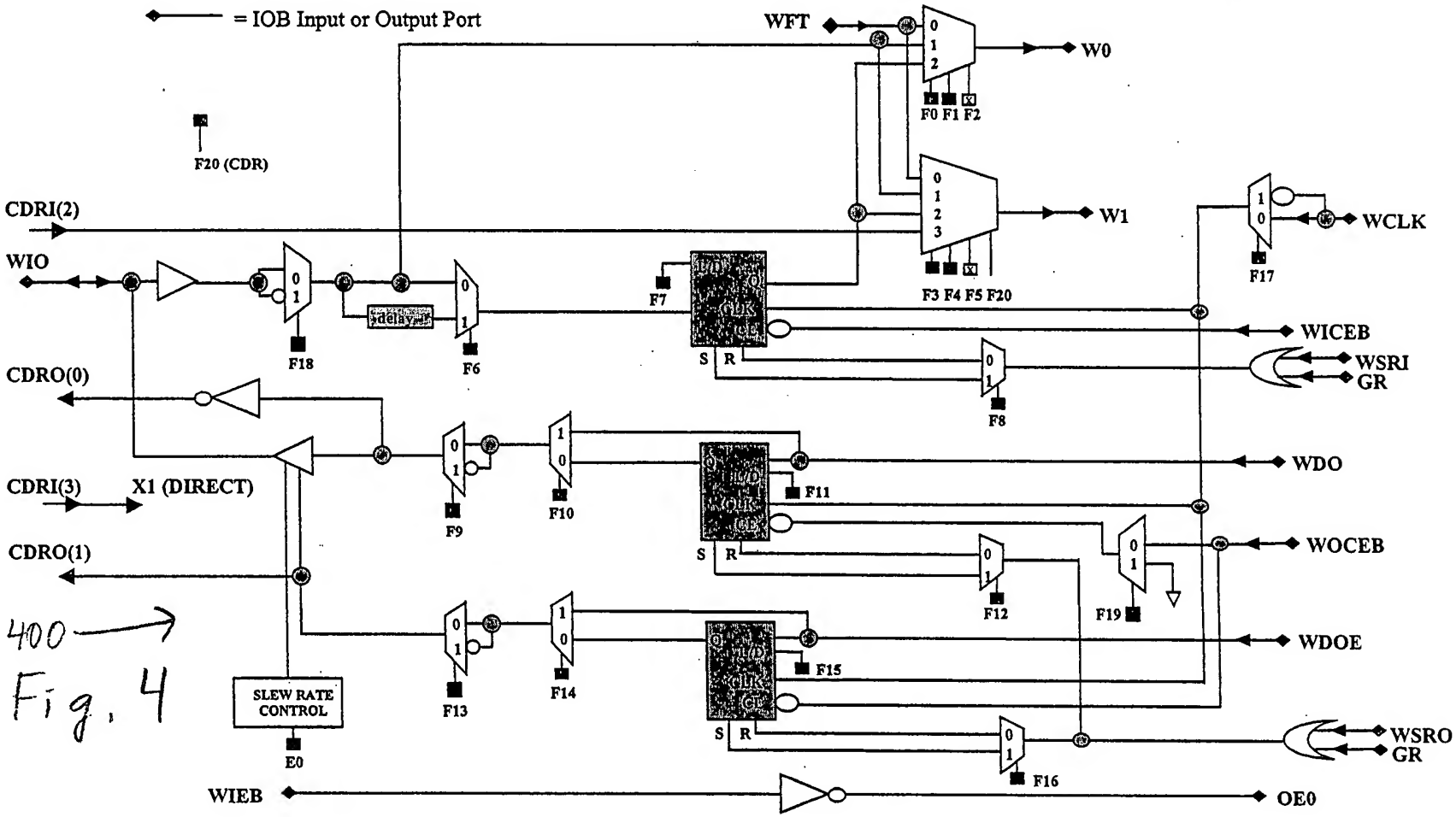
Fig. 2

200


WDOE
WDO
WCLK
WICEB
WOCEB
WSRI
WSRO
WFT
CDRI(0:3)
CDRO(0:3)
WIEB
ZIEB
WIO
ZIO
GR
IOBW(U)
302
IOG
304
IOBZ(U)
ZDOE
ZDO
ZCLK
ZICEB
ZOCEB
ZSRI
ZSRO
ZFT
W0
W1
OE0
X1
Y1
Z0
Z1
OE1
DIRECT CONNECTS
(W1, X1, Y1, Z1)
OSM
8
GENERAL
INTER-
CONNECT
306
2 OEs
2 Long Line Outputs
(W0, Z0)
To 3-state Shared Driver
= Globally Routable Port Symbol

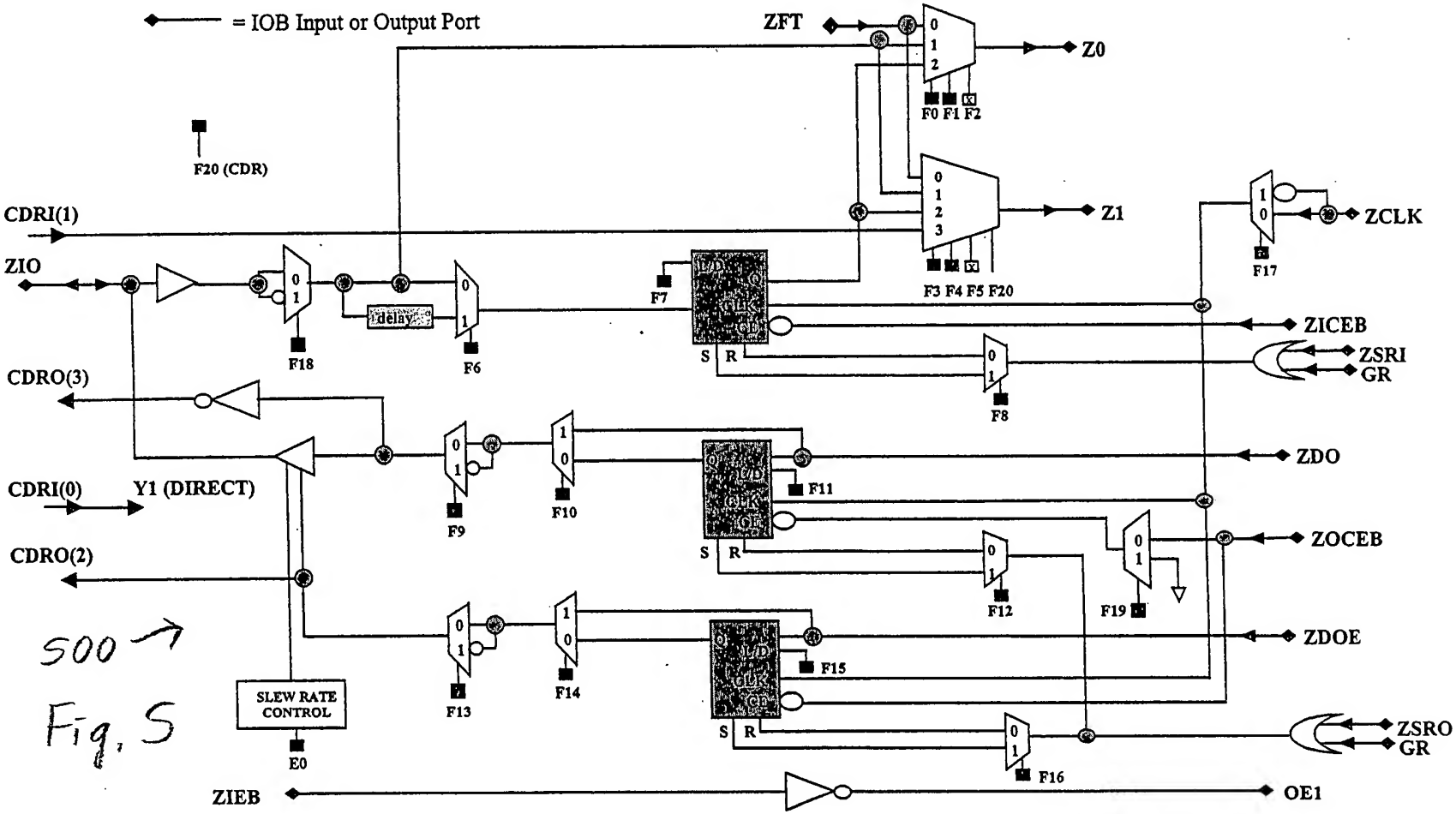
300

Fig. 3


= IOB Input or Output Port
WFT
W0
F0 F1 F2
F20 (CDR)
CDRI(2)
W1
F3 F4 F5 F20
WCLK
F17
WIO
F18
delay
F6
F7
WICEB
WSRI
GR
F8
CDRO(0)
WDO
CDRI(3)
X1 (DIRECT)
F9
F10
F11
WOCEB
CDRO(1)
F12
F19
WDOE
F13
F14
F15
SLEW RATE CONTROL
E0
WSRO
GR
F16
WIEB
OE0

400

Fig. 4


= IOB Input or Output Port
ZFT
Z0
F0 F1 F2
F20 (CDR)
CDRI(1)
Z1
F3 F4 F5 F20
ZCLK
F17
ZIO
F18
delay
F6
F7
F8
ZICEB
ZSRI
GR
CDRO(3)
ZDO
F9
F10
F11
CDRI(0)
Y1 (DIRECT)
CDRO(2)
ZOCEB
F12
F19
ZDOE
F13
F14
F15
SLEW RATE CONTROL
E0
F16
ZSRO
GR
ZIEB
OE1
500
Fig. 5

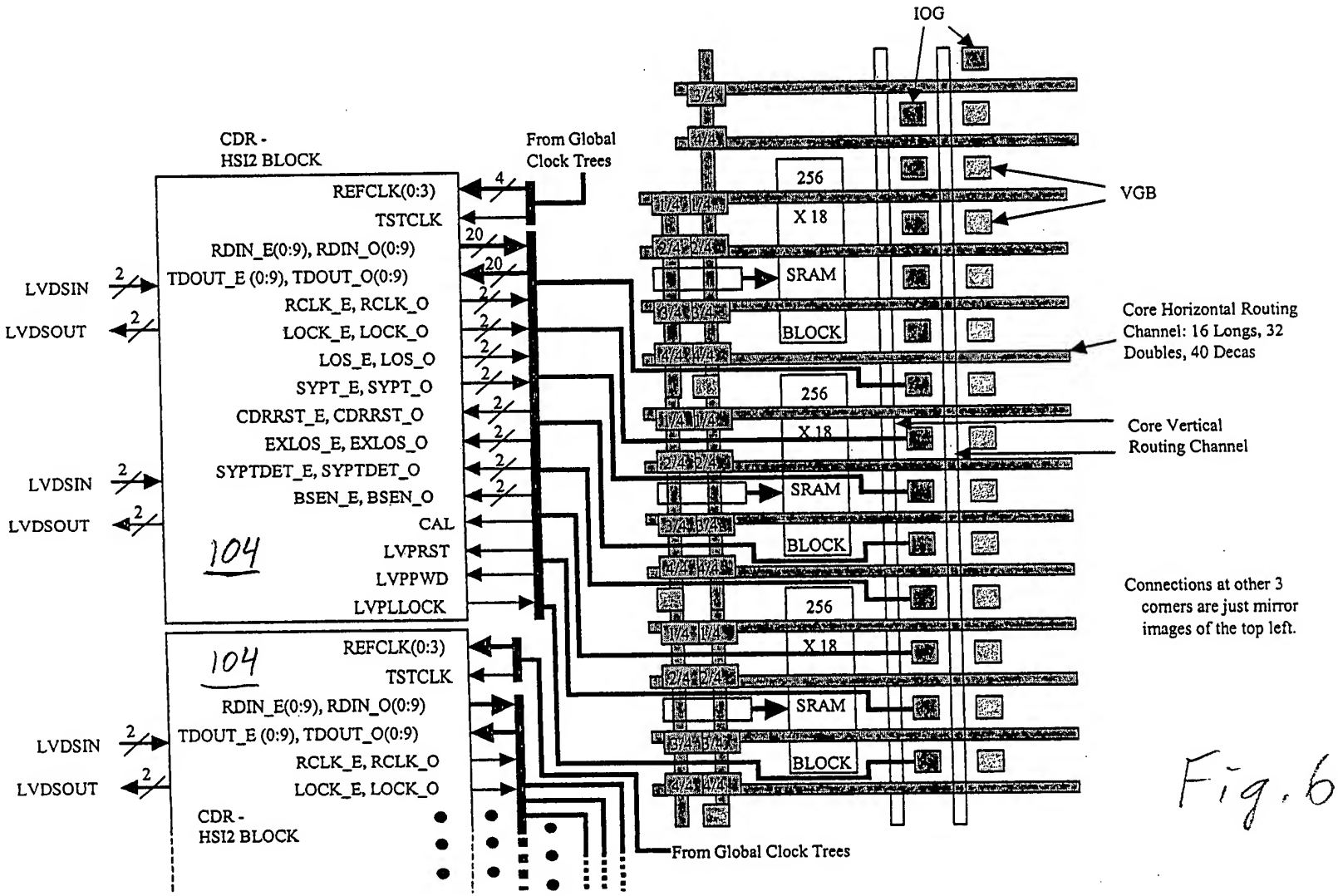

IOG
CDR -
HSI2 BLOCK
From Global
Clock Trees
REFCLK(0:3)
TSTCLK
RDIN_E(0:9), RDIN_O(0:9)
TDOUT_E (0:9), TDOUT_O(0:9)
RCLK_E, RCLK_O
LOCK_E, LOCK_O
LOS_E, LOS_O
SYPT_E, SYPT_O
CDRRST_E, CDRRST_O
EXLOS_E, EXLOS_O
SYPTDET_E, SYPTDET_O
BSEN_E, BSEN_O
CAL
LVPRST
LVPPWD
LVPLLOCK
LVDSIN
LVDSOUT
104
256
X 18
SRAM
BLOCK
VGB
Core Horizontal Routing
Channel: 16 Longs, 32
Doubles, 40 Decas
Core Vertical
Routing Channel
Connections at other 3
corners are just mirror
images of the top left.
From Global Clock Trees

Fig. 6

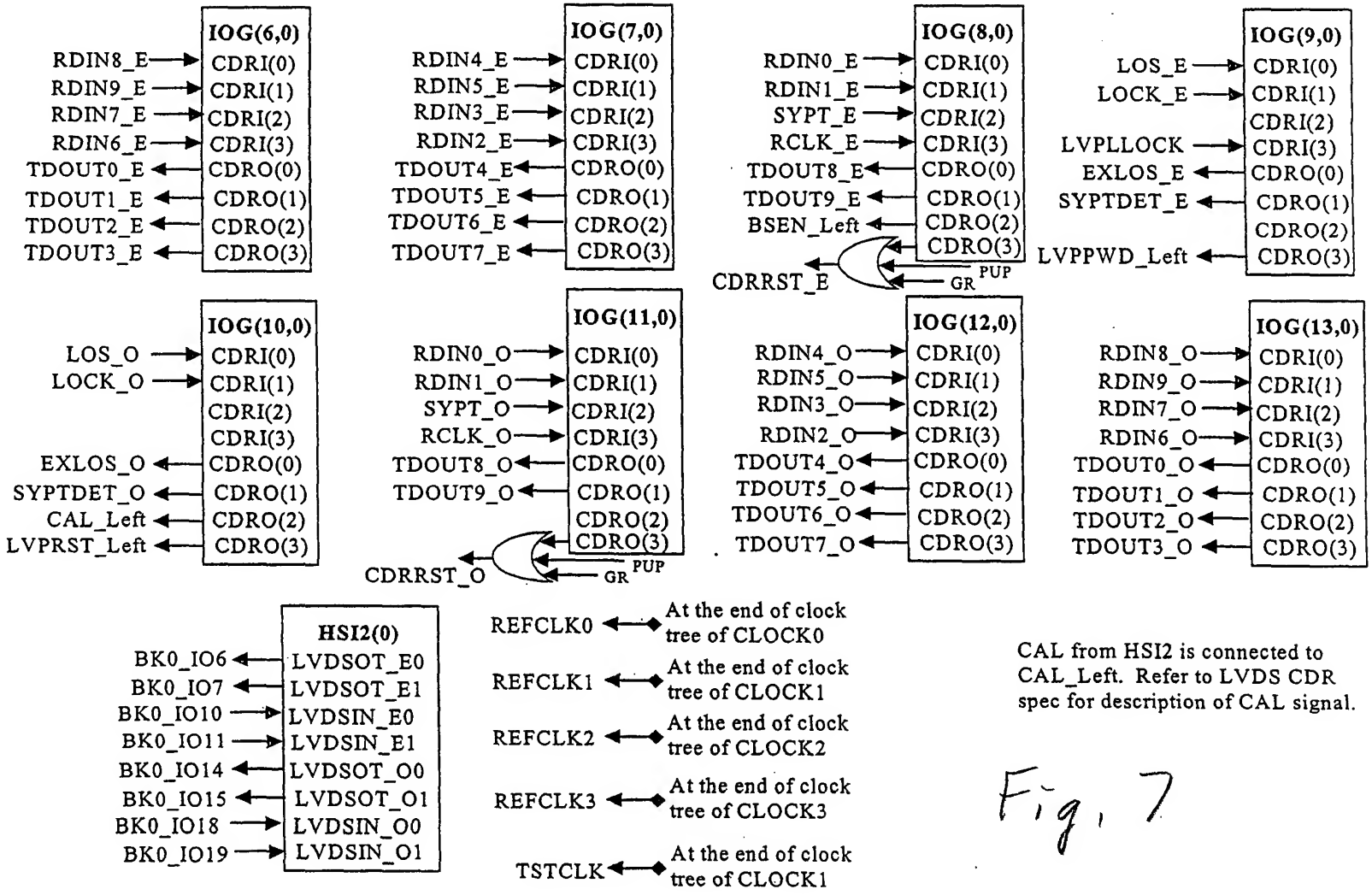

IOG(6,0)
RDIN8_E
RDIN9_E
RDIN7_E
RDIN6_E
TDOUT0_E
TDOUT1_E
TDOUT2_E
TDOUT3_E
CDRI(0)
CDRI(1)
CDRI(2)
CDRI(3)
CDRO(0)
CDRO(1)
CDRO(2)
CDRO(3)
IOG(7,0)
RDIN4_E
RDIN5_E
RDIN3_E
RDIN2_E
TDOUT4_E
TDOUT5_E
TDOUT6_E
TDOUT7_E
IOG(8,0)
RDIN0_E
RDIN1_E
SYPT_E
RCLK_E
TDOUT8_E
TDOUT9_E
BSEN_Left
CDRRST_E
GR
PUP
IOG(9,0)
LOS_E
LOCK_E
LVPLLOCK
EXLOS_E
SYPTDET_E
LVPPWD_Left
IOG(10,0)
LOS_O
LOCK_O
EXLOS_O
SYPTDET_O
CAL_Left
LVPRST_Left
IOG(11,0)
RDIN0_O
RDIN1_O
SYPT_O
RCLK_O
TDOUT8_O
TDOUT9_O
CDRRST_O
IOG(12,0)
RDIN4_O
RDIN5_O
RDIN3_O
RDIN2_O
TDOUT4_O
TDOUT5_O
TDOUT6_O
TDOUT7_O
IOG(13,0)
RDIN8_O
RDIN9_O
RDIN7_O
RDIN6_O
TDOUT0_O
TDOUT1_O
TDOUT2_O
TDOUT3_O
HSI2(0)
BK0_IO6
BK0_IO7
BK0_IO10
BK0_IO11
BK0_IO14
BK0_IO15
BK0_IO18
BK0_IO19
LVDSOT_E0
LVDSOT_E1
LVDSIN_E0
LVDSIN_E1
LVDSOT_O0
LVDSOT_O1
LVDSIN_O0
LVDSIN_O1
REFCLK0
REFCLK1
REFCLK2
REFCLK3
TSTCLK
At the end of clock tree of CLOCK0
At the end of clock tree of CLOCK1
At the end of clock tree of CLOCK2
At the end of clock tree of CLOCK3
At the end of clock tree of CLOCK1
CAL from HSI2 is connected to CAL_Left. Refer to LVDS CDR spec for description of CAL signal.

Fig. 7

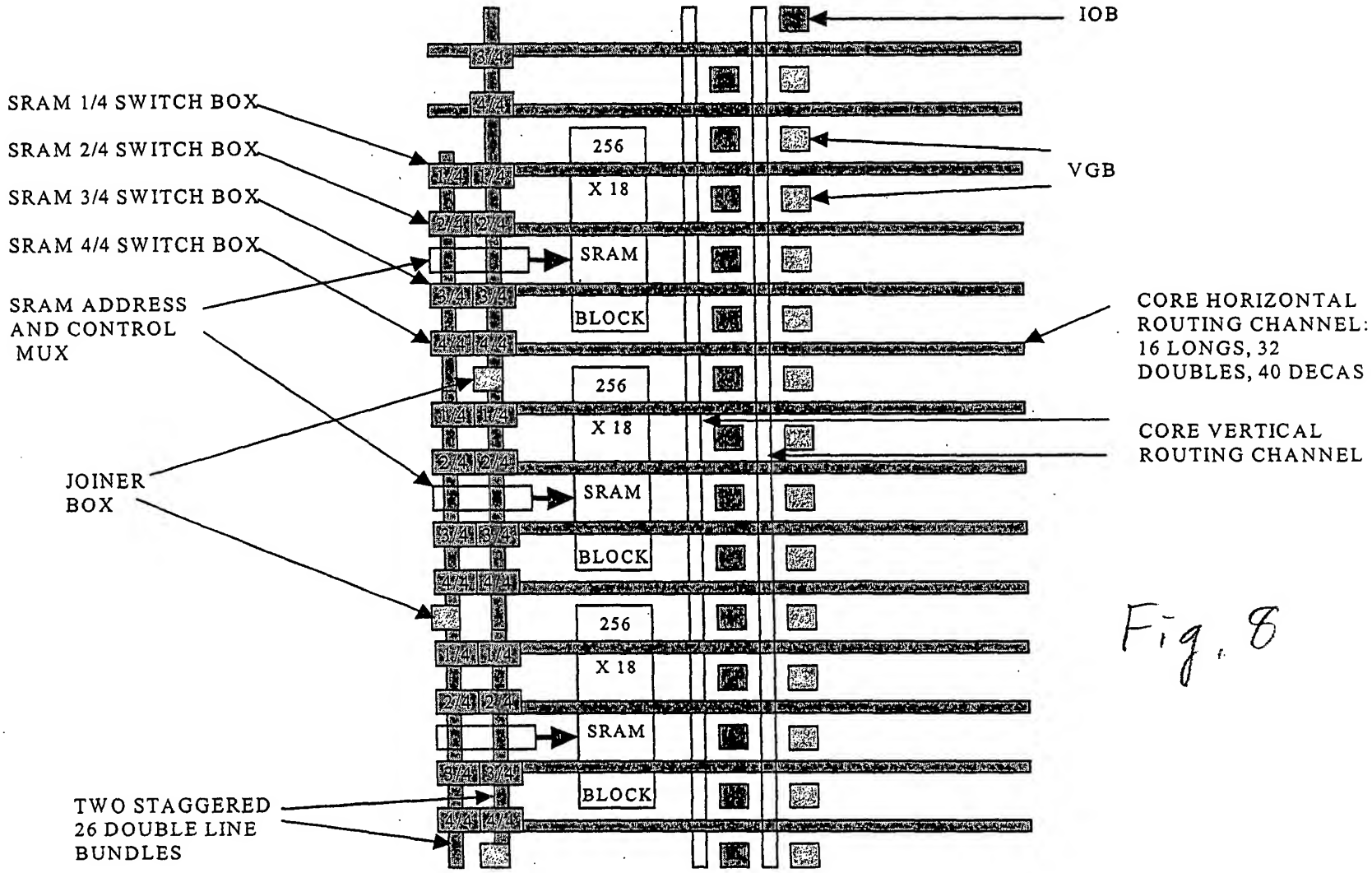

IOB
SRAM 1/4 SWITCH BOX
SRAM 2/4 SWITCH BOX
SRAM 3/4 SWITCH BOX
SRAM 4/4 SWITCH BOX
SRAM ADDRESS AND CONTROL MUX
JOINER BOX
TWO STAGGERED 26 DOUBLE LINE BUNDLES
256
X 18
SRAM
BLOCK
VGB
CORE HORIZONTAL ROUTING CHANNEL: 16 LONGS, 32 DOUBLES, 40 DECAS
CORE VERTICAL ROUTING CHANNEL

Fig. 8

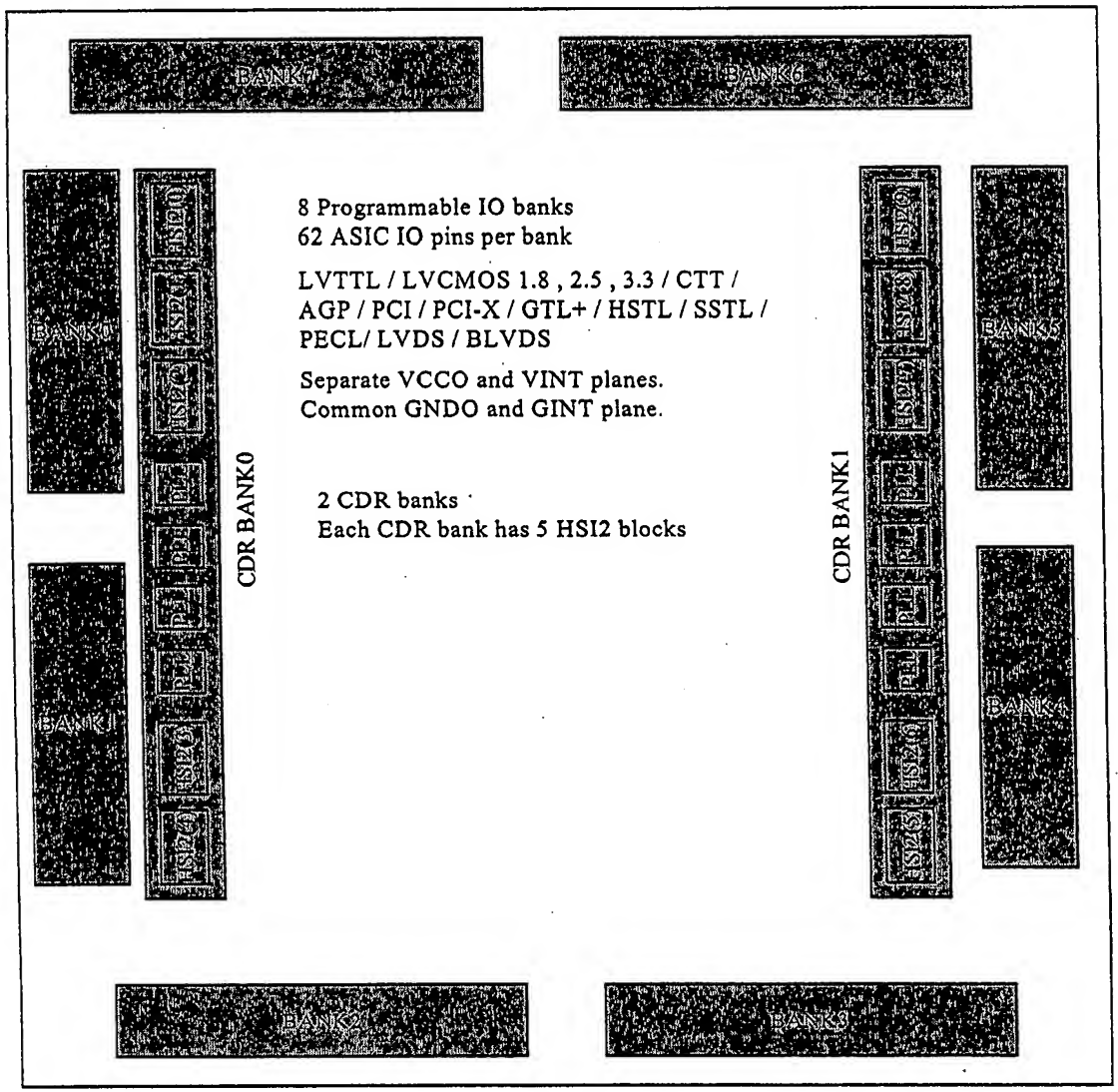

BANK7
BANK6
BANK0
BANK5
BANK1
BANK4
BANK2
BANK3
HSI2C0
HSI2C1
HSI2C2
HSI2C3
HSI2C4
HSI2S0
HSI2S1
HSI2S2
HSI2S3
HSI2S4
PLL
CDR BANK0
CDR BANK1
8 Programmable IO banks
62 ASIC IO pins per bank
LVTTL / LVCMOS 1.8 , 2.5 , 3.3 / CTT /
AGP / PCI / PCI-X / GTL+ / HSTL / SSTL /
PECL/ LVDS / BLVDS
Separate VCCO and VINT planes.
Common GNDO and GINT plane.
2 CDR banks
Each CDR bank has 5 HSI2 blocks

Fig. 9

LAVA1 (X-125 with 2X Memory Blocks, 22x22 GLB Array)

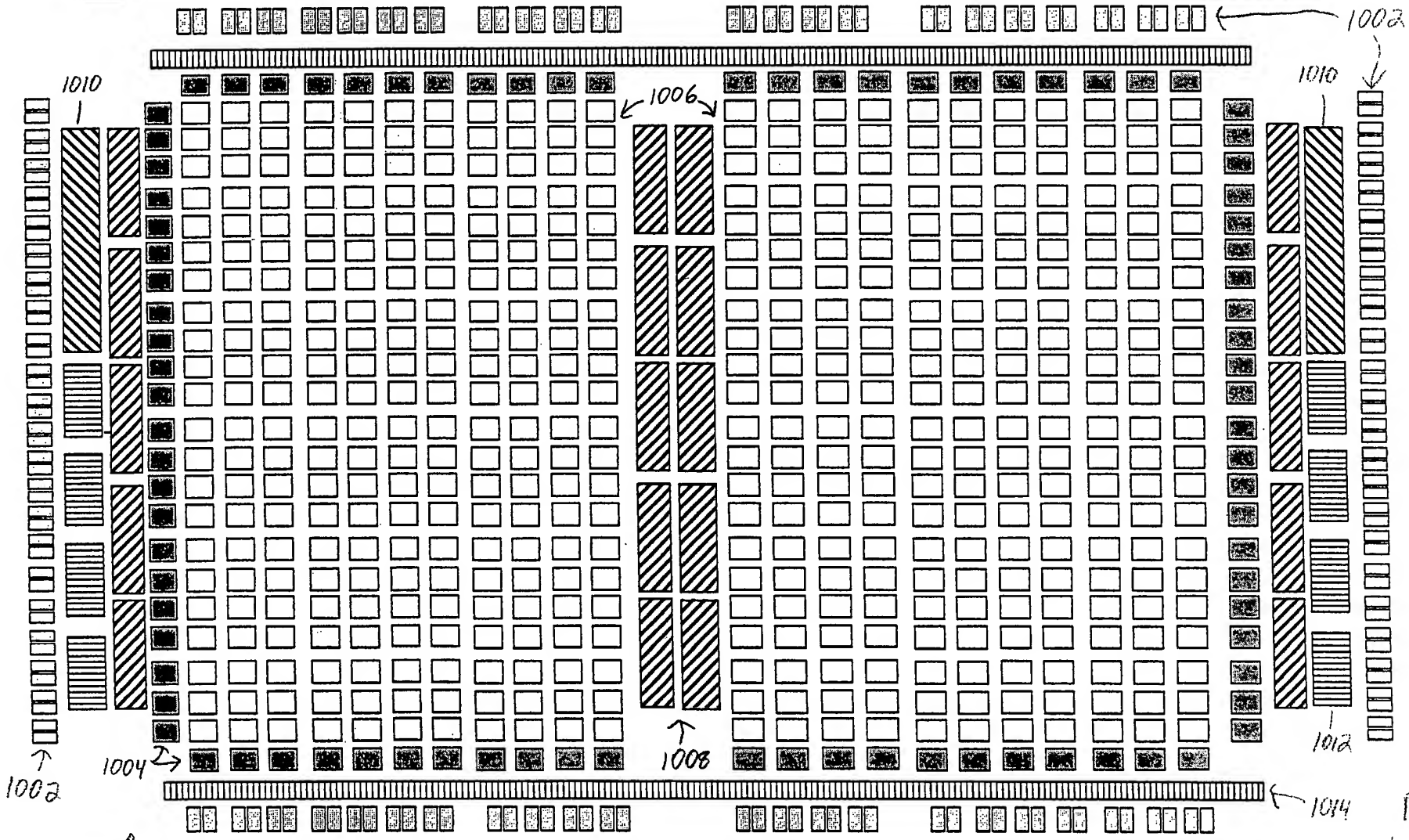


Fig. 10 484 GLBs,1936 LUTs, 176 IOs, 20 EMBs, 2 HSI2s, 8 PLLs

LAVA1 (X-1200 with 3X Memory Blocks, 62x62 GLB Array)

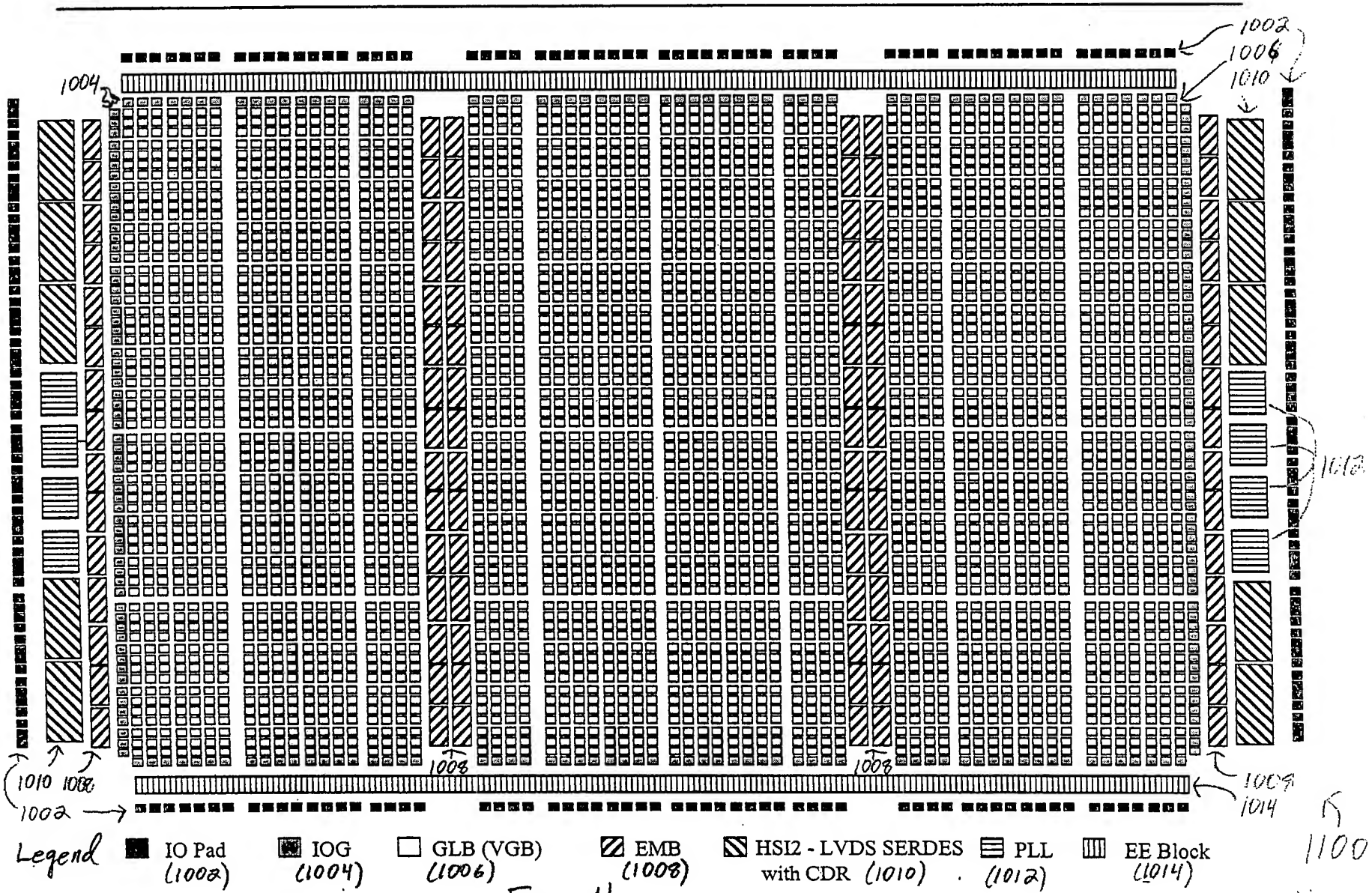


Fig. 11

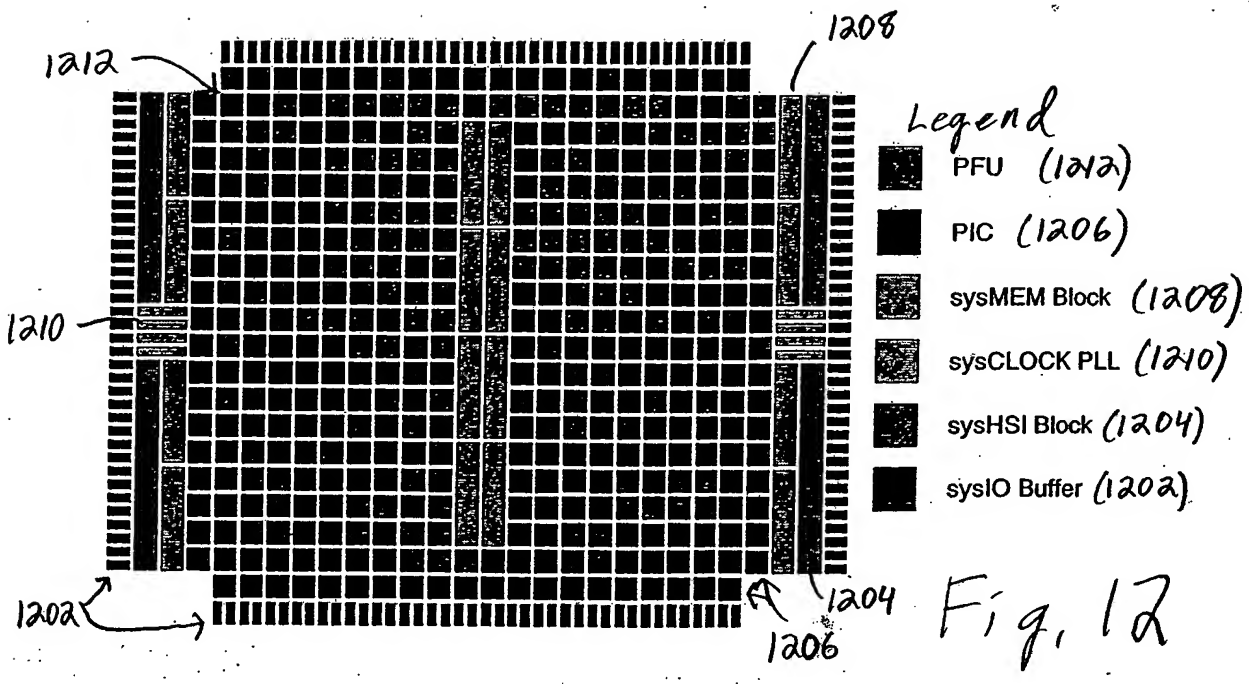

1212
1208
1210
1200
1202
1204
1206
Legend
PFU (1212)
PIC (1206)
sysMEM Block (1208)
sysCLOCK PLL (1210)
sysHSI Block (1204)
sysIO Buffer (1202)

Fig. 12

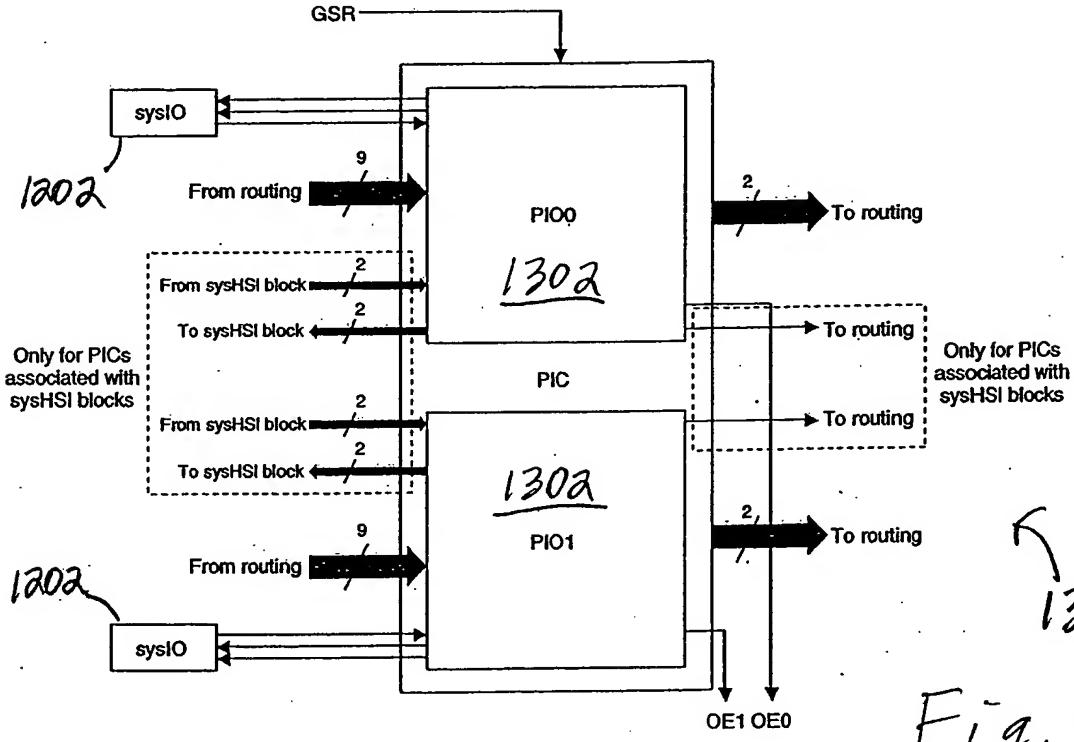

GSR
sysIO
1202
From routing
9
PIO0
1302
2
To routing
From sysHSI block
To sysHSI block
Only for PICs associated with sysHSI blocks
PIC
Only for PICs associated with sysHSI blocks
PIO1
1302
1300
OE1 OE0

Fig. 13

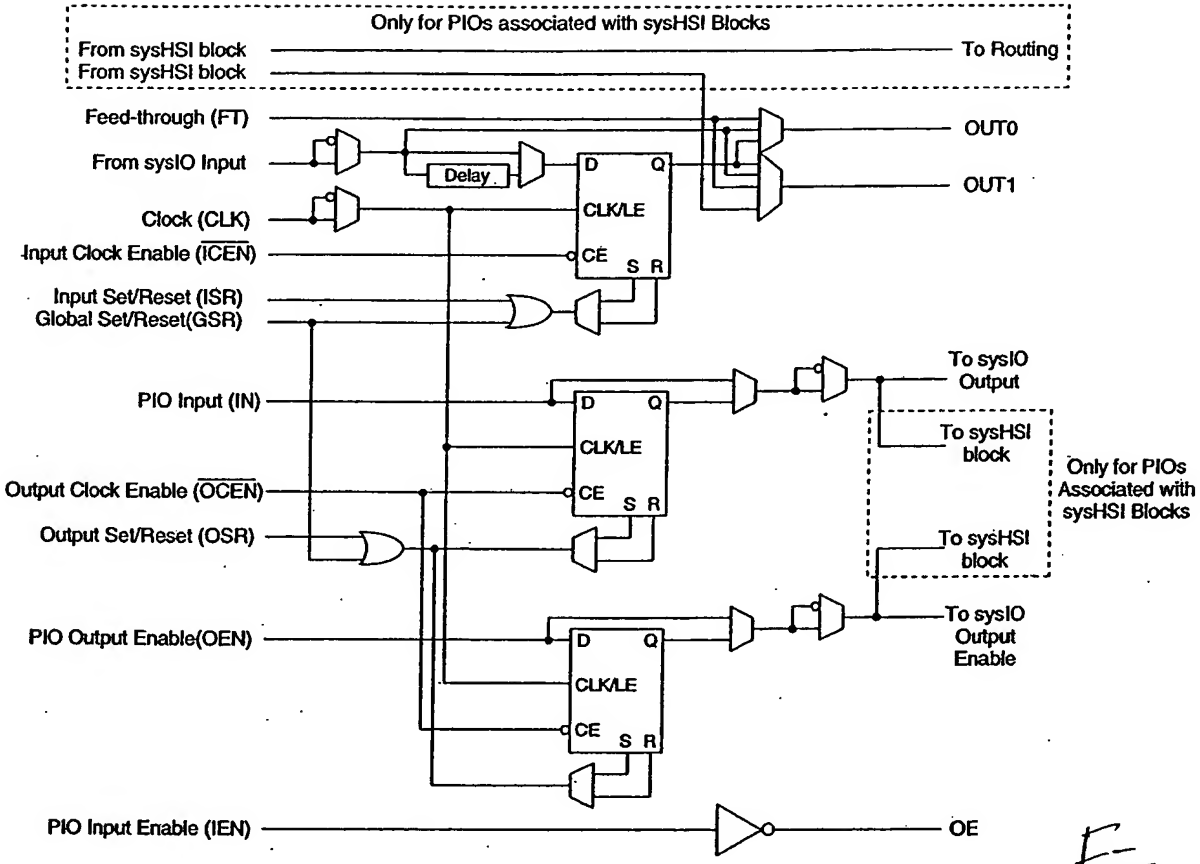

Only for PIOs associated with sysHSI Blocks
From sysHSI block
From sysHSI block
To Routing
Feed-through (FT)
From sysIO Input
Delay
D
Q
CLK/LE
CE
S R
OUT0
OUT1
Clock (CLK)
Input Clock Enable (ICEN)
Input Set/Reset (ISR)
Global Set/Reset(GSR)
PIO Input (IN)
To sysIO Output
To sysHSI block
Only for PIOs Associated with sysHSI Blocks
Output Clock Enable (OCEN)
Output Set/Reset (OSR)
To sysHSI block
PIO Output Enable(OEN)
To sysIO Output Enable
PIO Input Enable (IEN)
OE

Fig. 14

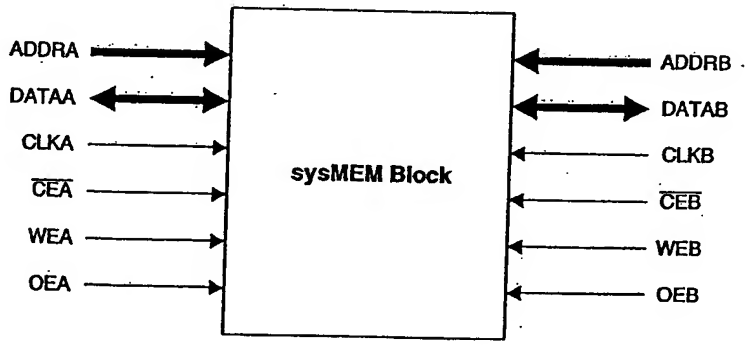

ADDRA
DATAA
CLKA
CEA
WEA
OEA
sysMEM Block
ADDRB
DATAB
CLKB
CEB
WEB
OEB

Fig. 15

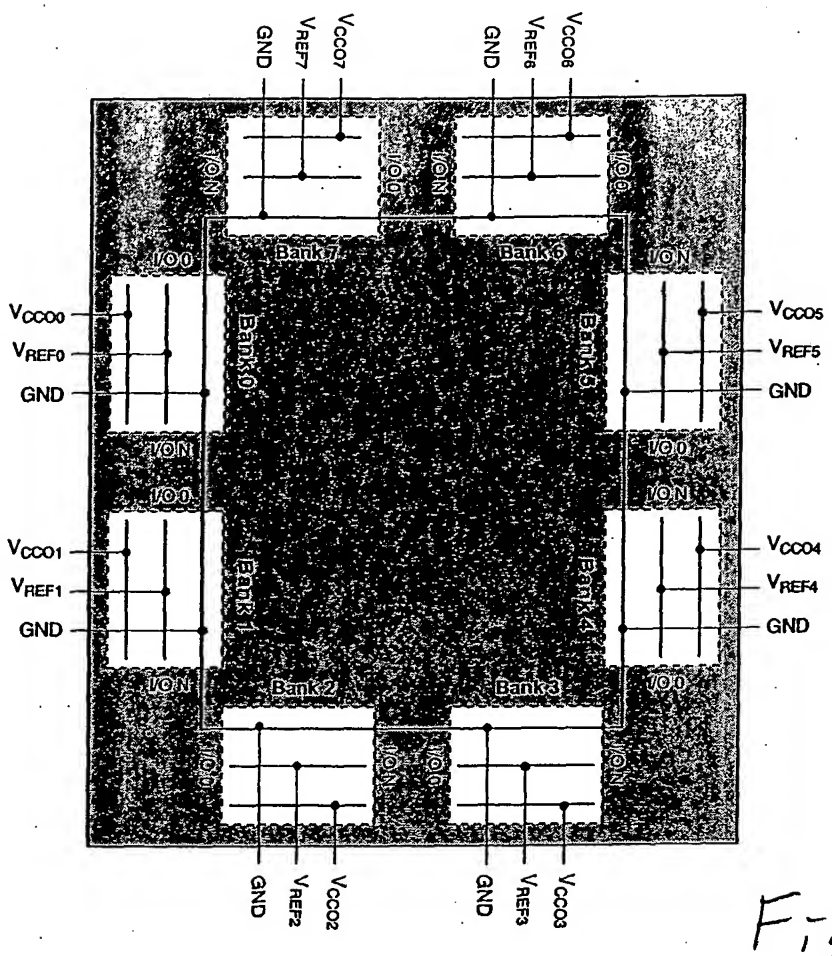

GND
VREF7
VCCO7
GND
VREF6
VCCO6
I/O N
I/O 0
Bank 7
Bank 6
VCCO0
VREF0
GND
Bank 0
Bank 5
VCCO5
VREF5
GND
VCCO1
VREF1
GND
Bank 1
Bank 4
VCCO4
VREF4
GND
Bank 2
Bank 3
GND
VREF2
VCCO2
GND
VREF3
VCCO3

Fig. 16

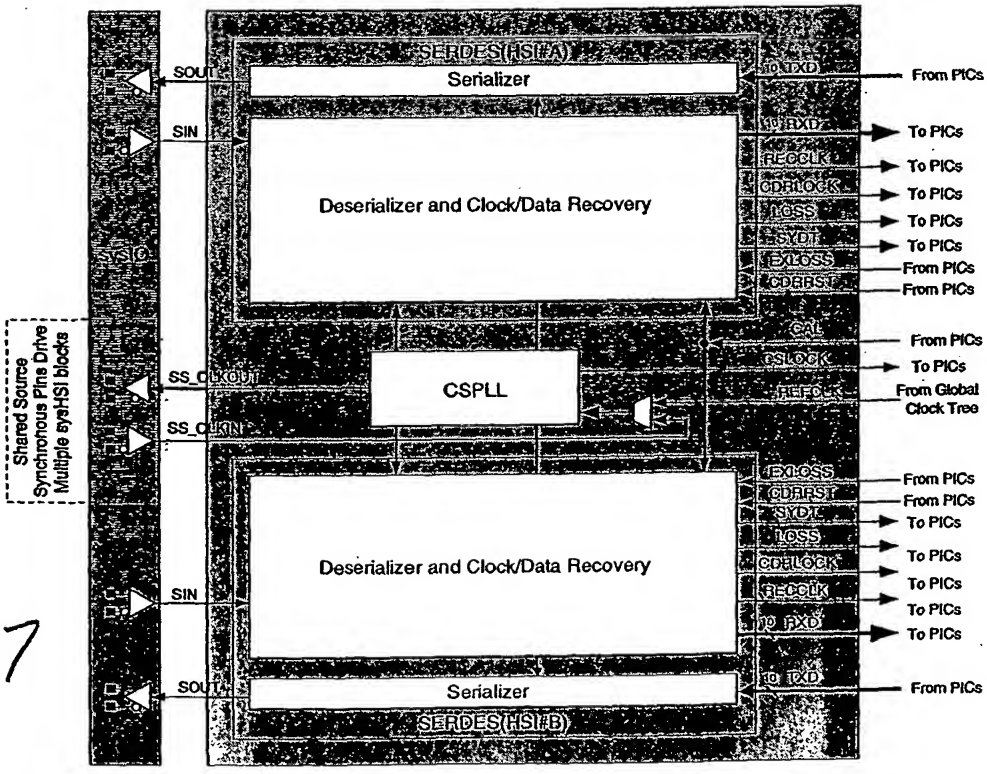

SERDES(HSI#A)
Serializer
SOUT
SIN
Deserializer and Clock/Data Recovery
SYSIO
SS_CLKOUT
SS_CLKIN
CSPLL
Shared Source Synchronous Pins Drive Multiple sysHSI blocks
Deserializer and Clock/Data Recovery
SIN
SOUT
Serializer
SERDES(HSI#B)
TXD
RXD
RECCLK
CDRLOCK
LOSS
SYDL
EXLOSS
CDRRST
CAL
CSLOCK
REFCK
From PICs
To PICs
From Global Clock Tree

Fig. 17